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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,918	11/26/2003	Jonathan Jedwab	10014224-1	1180

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EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	**PAPER NUMBER**
2133	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,918	JEDWAB ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

GUY LAMARRE
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Response to the applicant's amendment dated 12/8/2006
- Claims 1-35 have been submitted for examination
- Claims 1-35 have been rejected

Drawings Objections

1. In view of the applicant amended drawings filed on 12/8/2006; all objections to the drawings are withdrawn.

Response to Arguments

2. Applicant's arguments with respect to claims 1,9-12,19,25-27, 34 and 35 have been considered but are moot in view of the new ground(s) of rejection.

3. The indicated allowability of claims 2-8,13-18,20-24 and 28-33 are withdrawn in view of the newly discovered reference(s) to Brown et al. US patent no. 6360340 (Hereinafter Brown) and Yamada et al. US patent no. 6634004 (Hereinafter Yamada). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 12-14, 19,20, 25-28 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Brown et al. US patent no. 6360340 (Hereinafter Brown).

5. In regard to claim 1, Brown teaches:

- (Original) A magnetic memory, comprising:
- at least two magnetic memory cells configured to store data; and

(Note: col. 1, line 6 in Brown)

- a control system configured to at least twice obtain parametric values from the magnetic memory cells and generate a corresponding compressed fault map using the parametric values (note: col. 2, line 51), wherein at least one of the compressed fault maps is compared to a previous one of the compressed fault maps and an indication is provided if there are differences.

(Note: FIG.2, reference characters (210), (214), (216), (218), (220), (222) and (224) and col. 6, lines (7-37) in Brown)

6. In regard to claim 2, Brown teaches:

- (Original) The magnetic memory of claim 1, wherein each one of the compressed fault maps includes at least one error detection code (col. 3, lines (42-53) in Brown) result which is calculated over the addresses of the magnetic memory cells which have a fault, wherein each one of the magnetic memory cells has a corresponding one of at least two addresses, and wherein the one of the magnetic memory cells has the fault when a corresponding one of the parametric values is not within an expected range.

(Note: col. 5, lines 9-17 in Brown)

7. In regard to claim 25, Brown teaches:

- (Currently Amended) The magnetic memory of claim 1, wherein the control system means is configured to periodically obtain parametric values from the magnetic memory cells and generate a corresponding compressed fault map

(Note: FIG.2, reference characters (210), (214), (216), (218), (220), (222) and (224) and col. 6, lines (7-37) in Brown)

8. In regard to claim 26, Brown teaches:

- (Currently Amended) The magnetic memory of claim 25, wherein the control system means includes:
- first means configured to store a procedure for obtaining parametric values from the magnetic memory cells and generating the corresponding compressed fault map using the parametric values; and
- second means configured to periodically execute the procedure and generate the corresponding compressed fault map, wherein the second means compares the compressed fault map to a previous one of the compressed fault maps and provides the indication if there are differences.

(Note: FIG.2, reference characters (210), (214), (216), (218), (220), (222) and (224) and col. 6, lines (7-37) in Brown)

9. Claims 12, 27 and 34 are rejected for the same reasons as per claim 1.

10. Claims 13, 20 and 28 are rejected for the same reasons as per claim 2.

11. In regard to claim 14, Brown teaches:

- (Original) The controller of claim 13, wherein the first compressed fault map and the second compressed fault map each include at least two error detection code results, wherein each one of the error detection code results is calculated for a corresponding one of at least two address ranges, over the addresses of the magnetic memory cells which have the fault and are within a same one of the address ranges, wherein each one of the addresses is within only one of the address ranges.

(Note: col. 5, lines (8-17) in Brown)

12. In regard to claim 19, Brown teaches:

- (Original) A storage system, comprising:
- at least two magnetic memory storage devices, each including at least one array of magnetic memory cells configured to store data; and

(Note: col. 7, line 28 in Brown)

- a control system configured to periodically obtain parametric values from magnetic memory cells in the magnetic memory storage devices and generate, using the parametric values, at least one error detection code result which is compared to a previous at least one error detection code result, wherein an indication is provided if there are differences.

(Note: FIG.2, reference characters (210), (214), (216), (218), (220), (222) and (224) and col. 6, lines (7-37) in Brown)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. Claims 3-11,15-18, 21-24, 29-33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown as applied to claim 2 above, and further in view of Yamada et al. US patent no. 6634004 (Hereinafter Yamada).

14. In regard to claim 3 Brown substantially teaches all the limitations as in claim 2.

However, Brown does teach:

- (Original) The magnetic memory of claim 2, wherein each one of the compressed fault maps includes at least two error detection code

results, wherein each one of the error detection code results is calculated for a corresponding one of at least two address ranges, over the addresses of the magnetic memory cells which have the fault and are within a same one of the address ranges, wherein each one of the addresses is within only one of the address ranges.

Yamada, in analogous art that teach threshold analysis system capable of deciding all threshold voltages included in memory device teaches:

- (Original) The magnetic memory of claim 2, wherein each one of the compressed fault maps includes at least two error detection code results, wherein each one of the error detection code results is calculated for a corresponding one of at least two address ranges (Note: fig. 3, and col. 4, lines (51-67) in Yamada) , over the addresses of the magnetic memory cells which have the fault and are within a same one of the address ranges, wherein each one of the addresses is within only one of the address ranges.

(Note Fig. 3 address ranges in Yamada)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Brown that comprise of fault maps error diction code with the teaching of Dillon.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need to efficiently calculate parametric values of a memory

devices.

15. In regard to claim 4, Yamada teaches:

- (Original) The magnetic memory of claim 1, wherein each one of the compressed fault maps includes at least one error detection code result which is calculated over fault types and corresponding addresses of the magnetic memory cells which have a fault, wherein each one of the magnetic memory cells has a corresponding one of at least two addresses, wherein the one of the magnetic memory cells has the fault when a corresponding one of the parametric values is not within an expected range, and wherein the corresponding one of the parametric values is compared to the expected range to infer a corresponding one of the fault types.

(Note: Figures 4 and 5 in Yamada)

16. In regard to claim 5, Yamada teaches:

- (Original) The magnetic memory of claim 4, wherein each one of the compressed fault maps includes at least two error detection code results, wherein each one of the error detection code results is calculated over one of the fault types and the corresponding addresses of all of the magnetic memory cells which have a same one of the fault types.

(Note: Figure 5, any of fail bit information "X" in Yamada)

17. Claims 6, 24, 29 and 32 are rejected for the same reasons as per claim 3.

18. In regard to claim 7, Yamada teaches:

- (Original) The magnetic memory of claim 4, wherein the fault types and the corresponding addresses of the magnetic memory cells are sorted into a numerical order before the error detection code result is calculated.

Note the sequence of threshold information faults of device under test in FIG. 5.

19. In regard to claim 8, Yamada teaches

- (Original) The magnetic memory of claim 4, wherein the fault types and the corresponding addresses of the magnetic memory cells are sorted into a numerical order before the error detection code result is calculated.

(Note: col. 7, lines 3-55) in Yamada)

20. In regard to claim 9, Brown teaches:

- (Original) The magnetic memory of claim 4, wherein the error detection code result is calculated using a cyclic redundancy check code.

Note: the RLE "Run Length Encoder" in FIG. 2, reference character (216) in Brown produces fault signature code. The CRC code is a design choice that is obvious over Brown.

21. In regard to claim 10, Yamada teaches:

- (Original) The magnetic memory of claim 1, wherein the previous one of the compressed fault maps is generated using parametric values

obtained from the magnetic memory cells the first time that the control system obtains the parametric values from the magnetic memory cells.

(Note: FIG. 4, reference characters (s12), (s14) and (s16) in Yamada)

21. In regard to claim 11, Brown teaches:

- (Original) The magnetic memory of claim 1, wherein the previous compressed fault map is stored in at least one of the magnetic memory cells.

(Note: FIG. 1, reference character (126) in Brown)

23. Claims 15, 22, 30, and 33 are rejected for the same reasons as per claim 4.

24. Claims 16, 23 and 31 are rejected for the same reasons as per claim 5.

25. Claims 17 and 21are rejected for the same reasons as per claim 3.

26. Claim 18 is rejected for the same reasons as per claim 11.

27. Claim 35 is rejected for the same reasons as per claim 7.

Conclusion

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Takano et al. US patent teaches failure analysis memory for semiconductor memory testing devices and its storage method.
- Yumoto US publication no. 2002/0031017 teaches nonvolatile semiconductor memory device and test method with memory assisted roll call.

- Voshell US patent no. 6842874 teaches method and apparatus for redundant location addressing using data compression.
- Bula et al. US patent 5317573 teaches apparatus and method for real time data error capture and compression redundancy analysis.
- Bunker US patent 6311299 teaches data compression circuit and method for testing embedded memory devices.
- Ryan US patent 4456995 teaches apparatus for high speed fault mapping of large memories.
- Hoffman et al. US publication no. 2006/0242492 teaches method and apparatus for masking known fails during memory tests readout.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2133

3/1/07